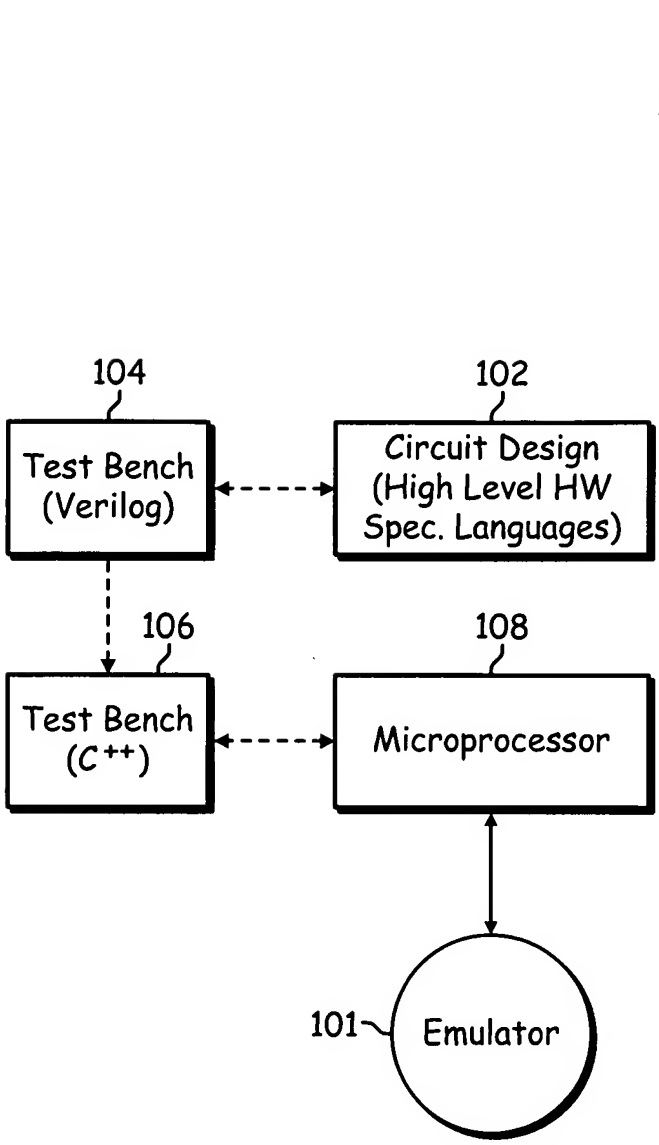
100
104
102
Test Bench
(Verilog)
Circuit Design
(High Level HW
Spec. Languages)
106
108
Test Bench
(C++)
Microprocessor
101
Emulator

FIG. 1

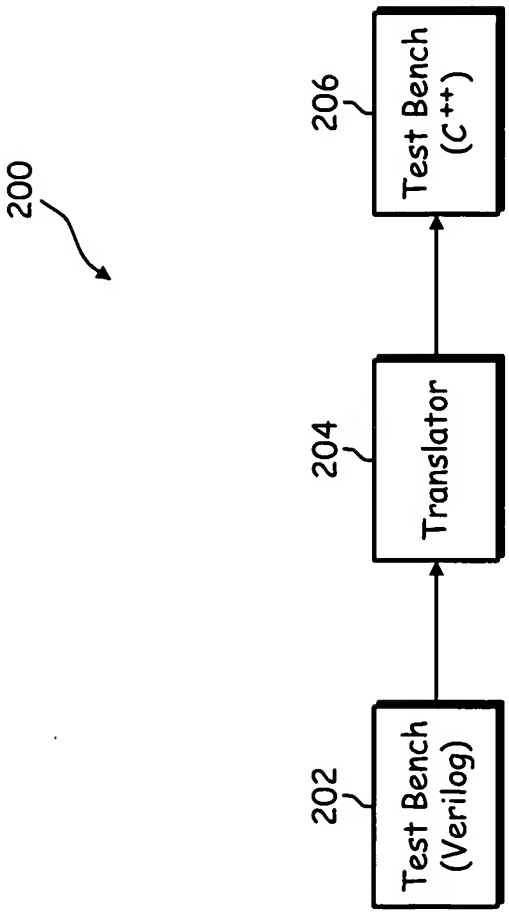

FIG. 2

VERILOG PATTERN	C++ PATTERN / ACTION
# Delay Statements	Remove # Delay Statements
` idef Statements	Translate `idef Statements
` Symbols	Remove ` Symbols
Begin	{
End	}
Register Definitions	Convert Register Definitons
Combinatorial Assignments	Convert Combinatorial Assignments
Events	Convert Events
Verilog Switches	Convert Verilog Switches
Verilog Concat Expressions	Convert Verilog Concat Expressions
Verilog Parameters	Convert to C++ #Defines
Verilog Consts	Convert to C Consts
Verilog Bit Access Macro	Convert Bit Access Macro

FIG. 3

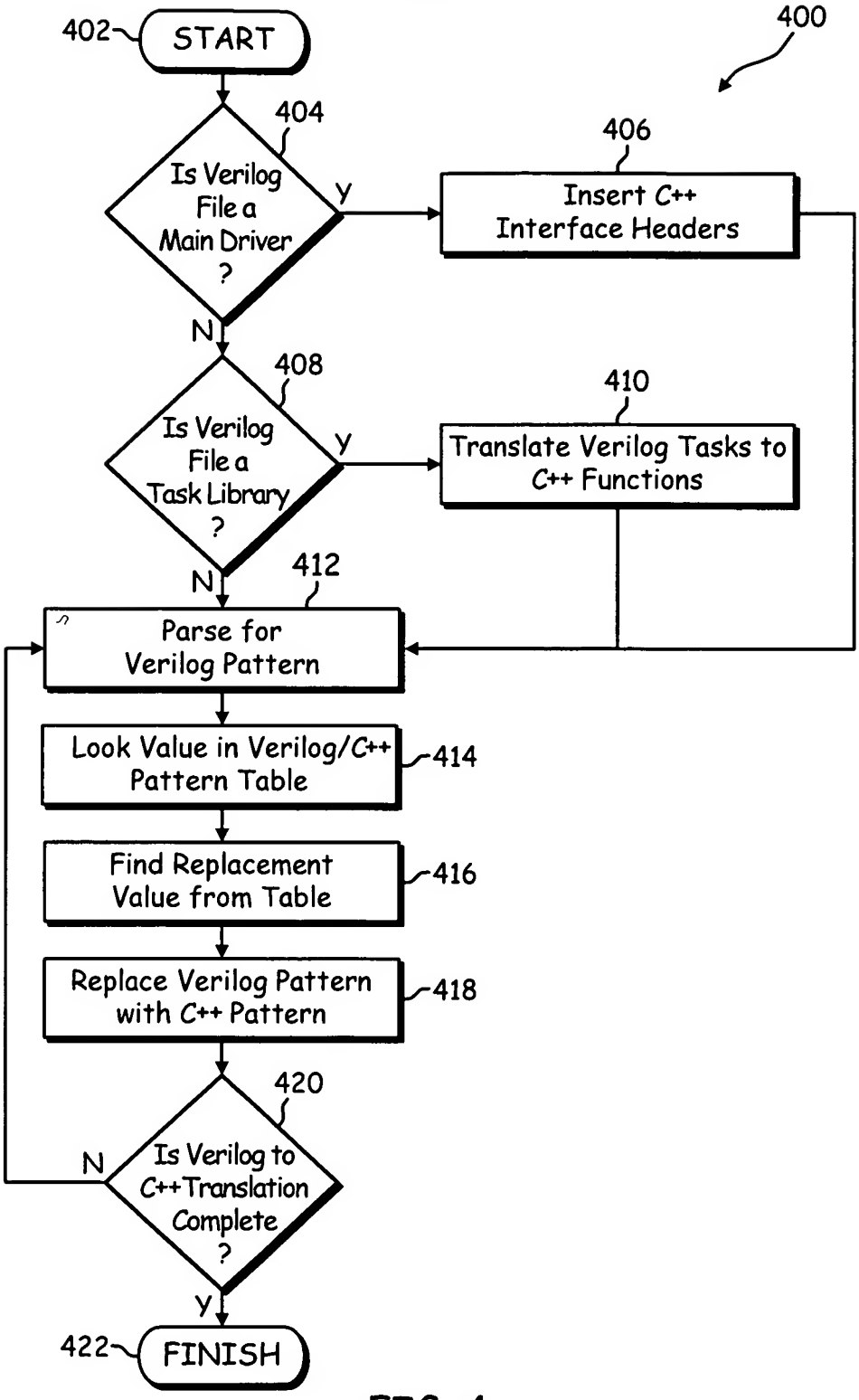
400
402
START
404
Is Verilog File a Main Driver ?
Y
406
Insert C++ Interface Headers
N
408
Is Verilog File a Task Library ?
Y
410
Translate Verilog Tasks to C++ Functions
N
412
Parse for Verilog Pattern
Look Value in Verilog/C++ Pattern Table
414
Find Replacement Value from Table
416
Replace Verilog Pattern with C++ Pattern
418
420
N
Is Verilog to C++Translation Complete ?
Y
422
FINISH

FIG. 4

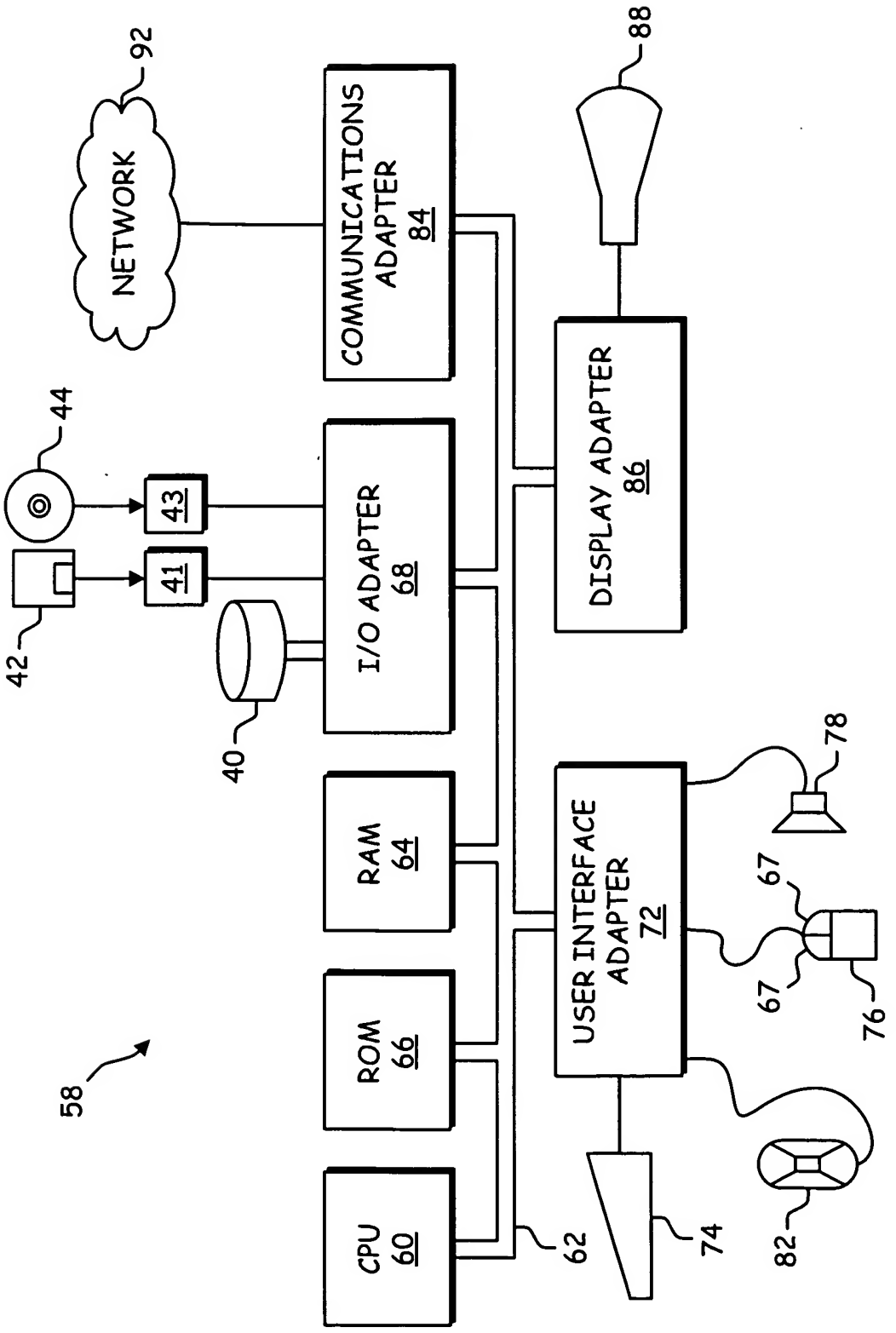
58
CPU 60
ROM 66
RAM 64
I/O ADAPTER 68
COMMUNICATIONS ADAPTER 84
NETWORK
92
DISPLAY ADAPTER 86
88
USER INTERFACE ADAPTER 72
62
74
82
67
67
76
78
40
42
41
43
44

FIG. 5